## What is claimed is:

- 1. An integrated circuit, comprising:
- an array of ferroelectric memory cells, each cell having a capacitor stack having a ferroelectric core with a crystallization in the (001) family, the ferroelectric cores having asymmetric domains, wherein at least about 40% of the domains are functionally oriented with respect to the capacitor stack.
- 2. The integrated circuit of claim 1, wherein from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack.
- 3. The integrated circuit of claim 1, wherein the ferroelectric cores are PZT cores and the PZT of each core has a switched polarization of at least about  $60 \,\mu\text{C/cm}^2$ .

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4. The integrated circuit of claim 1, further comprising:
a dielectric layer covering the array of memory cells, the dielectric layer having a metal filled via over each ferroelectric core, the vias each having a cross section about as large or larger than that of the ferroelectric cores.

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5. The integrated circuit of claim 1, wherein electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick.

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- 6. The integrated circuit of claim 1, wherein the capacitor stacks are formed over metal filled vias, the vias each having a cross section near their top that is about as large or larger than that of the ferroelectric cores.
  - 7. A method of manufacturing an integrated circuit, comprising:

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forming an array of ferroelectric memory cells on a semiconductor substrate, the ferroelectric memory cells having ferroelectric cores, the ferroelectric cores having a Curie temperature;

bringing the substrate to a temperature near a Curie temperature of the ferroelectric cores.

subjecting the substrate to a temperature program, whereby thermally induced stresses on the ferroelectric cores cause a switched polarization of the cores to increase by at least about 25% as the cores cool to about room temperature.

completing the processing of the substrate without raising the temperature above the Curie temperature.

- 8. The method of claim 7, wherein the ferroelectric cores comprise PZT and the temperature program comprises keeping the ferroelectric cores within about 100 °C of the Curie temperature for at least about 40 minutes.
- 9. The method of claim 7, wherein the ferroelectric cores comprise PZT and the temperature program comprises keeping the ferroelectric cores within about 100 °C of the Curie temperature for at least about 100 minutes.
- 10. The method of claim 7, wherein the ferroelectric cores comprise PZT and the temperature program comprises keeping the ferroelectric cores within about 50 °C of the Curie temperature for at least about 50 minutes.
- 11. The method of claim 7, wherein the ferroelectric cores comprises PZT and are formed at a temperature of at least about 600 °C.
- 12. The method of claim 7, wherein the ferroelectric cores are in capacitor stacks formed over metal filled vias and the vias each have a cross

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section near their top that is about as large or larger than that of the ferroelectric cores.

- 13. The method of claim 7, wherein over the array of memory cells there is a layer comprising dielectric having a via over each memory cell, the vias being filled with a metal and each via having an area greater than or equal to the area of the ferroelectric core of the underlying memory cell.
- 14. The method of claim 7, wherein an electrode adjacent the ferroelectric cores comprises iridium and is at least about 200 nm thick.
  - 15. An integrated circuit, comprising:
    an array of ferroelectric memory cells, having ferroelectric cores;
    and

over the array of memory cells, a layer comprising dielectric having a via over each memory cell, the vias being filled with a metal and each via having an area greater than or equal to the area of the ferroelectric core of the underlying memory cell.

- 16. The integrated circuit of claim 15, wherein electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick.
- 17. The integrated circuit of claim 15, wherein the ferroelectric cores are in capacitor stacks formed over metal filled vias, the vias each having a cross section near their top that is about as large or larger than that of the ferroelectric cores.

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- 18. The integrated circuit of claim 15, wherein the ferroelectric cores are in capacitor stacks and comprise domains and at least about 40% of the domains are functionally oriented with respect to the capacitor stack.
- 19. The integrated circuit of claim 15, wherein the ferroelectric cores are in capacitor stacks and comprise domains and from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack
- 20. The integrated circuit of claim 15, wherein the ferroelectric cores are PZT cores and the PZT of each core has a switched polarization of at least about  $60 \,\mu\text{C/cm}^2$ .

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